UNITED STATES PATENT AND TRADEMARK OFFICE

H'D

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,639	09/09/2003	Han-Lim Lee	5000-1-433	4713

33942 7590 02/19/2008

CHA & REITER, LLC
210 ROUTE 4 EAST STE 103
PARAMUS, NJ 07652

EXAMINER
LIU, LI

ART UNIT	PAPER NUMBER
2613	

MAIL DATE	DELIVERY MODE
02/19/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,639	LEE ET AL.	
	Examiner	Art Unit	
	Li Liu	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/13/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/29/2007 has been entered.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11/13/2007 is being considered by the examiner.

Response to Arguments

3. Applicant's arguments filed 10/26/2007 have been fully considered but they are not persuasive. The examiner has thoroughly reviewed Applicant's amendment and arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation.

Applicant's argument – "The combination of Ono and Kitajima would not create a device that generates an output having a phase that is correlated with the output of the T-flip-flop, as recited in the amended claims". "For example, with a D-flip-flop the Q output always takes on the state of the D input at the moment of a rising clock edge,

and never at any other time. Thus, the Q output takes the value of the D input and delays it by one clock count. The T-flip-flop, on the other hand, is a frequency divider that divides the clock input by two. Thus, the output of the T-flip flop incorporated into Fig. 18 of Ono would cause the output signal to have a frequency of one-half that of the input NRZ signal". "Hence, the incorporation of the T-flip-flop in the teaching of Ono alters the principles of the teachings of Ono and as such would render Ono unfit for the purpose for which it was designed".

Examiner's response – It not quite clear what frequency the applicant refers to when the applicant argue "the output signal to have a frequency of one-half that of the input **NRZ signal**". As clearly shown in Figure 8 of Kitajima and the Figure 16 of new cited prior art of Wei et al, the data rate of the electrical signal from the T-FF does not change. In Fig. 18, Ono uses the D-FF 39 with the precoder 7 to drive the single modulator to get both intensity modulation and phase modulation so to generate a duobinary optical signal. The D-FF needs the precoder so to generate the proper electrical drive signal. For Fig. 18, just replace the D-FF **only** by T-FF is "render Ono unfit for the purpose for which it was designed". However, the precoder in Figures 8, 13, 23 is replaceable by the T-FF, so that a T-FF is used to drive the phase modulator. It is also well known to one skilled in the art that a T flip-flop can be built using D flip-flop.

As disclosed by Kitajima et al and Wei et al, the T flip-flop is triggered in response to a rise-up edge of the input signal to thereby produce an output signal (e.g., at one output) having a waveform such as illustrated in following Figure O1 (the Output from T-FF Q Port), this electrical signal separates "1" bit values in the sequence of the

NRZ electrical signal into first groups of "1" bit values (e.g., the group of "1" at the odd position) and second groups of "1" bit values (e.g., the group of "1" at the even position). The first group of "1" is "represented/drived" by the electrical signal with intensity of "1" in the output of T-FF Q-Port, the second group of "1" is "represented/drived" by the electrical signal with intensity of "0" in the output of T-FF Q-Port.

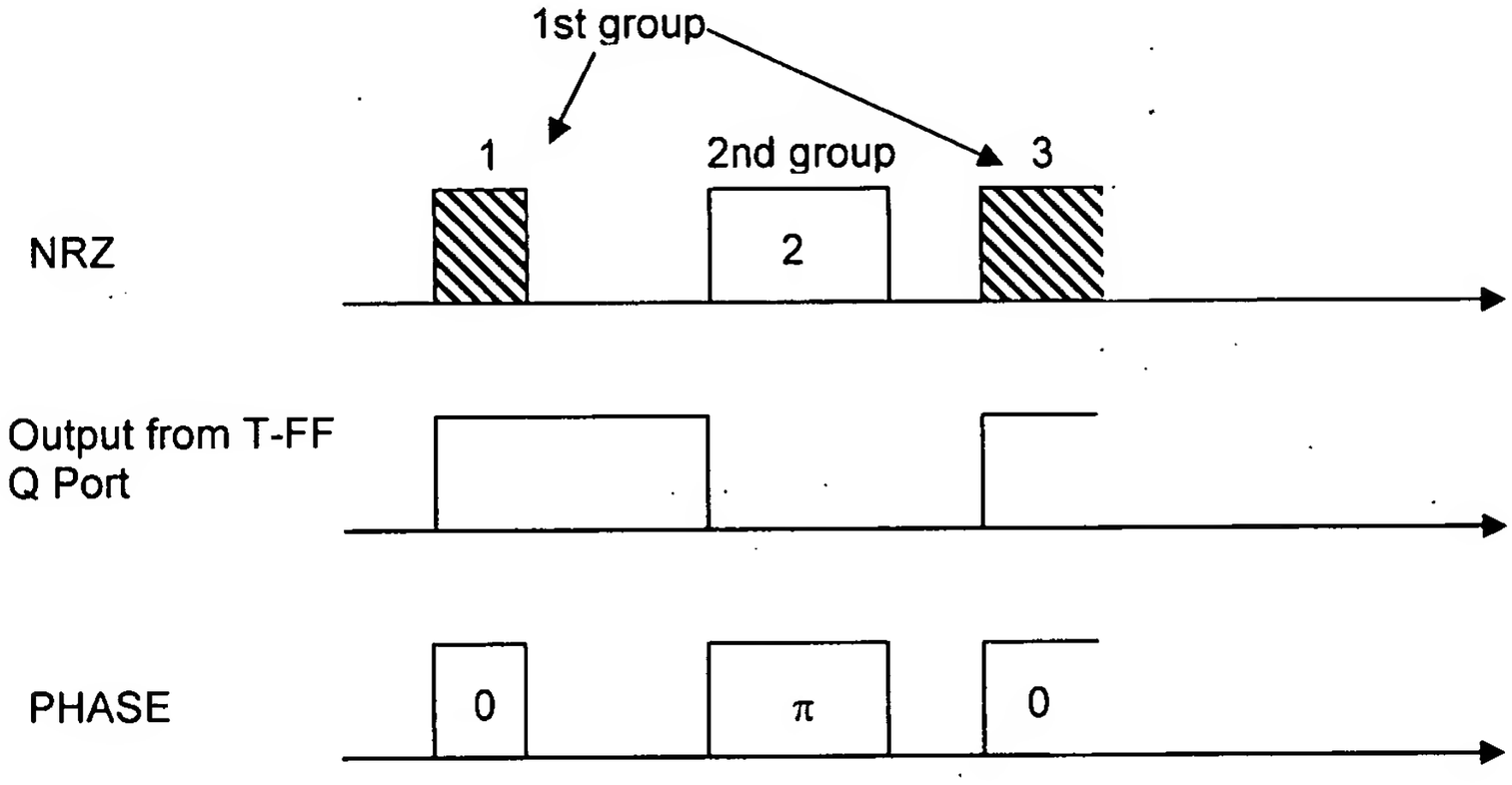

Figure O1

Ono et al teaches that the phase of the output signal from the duobinary modulators depends on the drive signal from the precoder (column 7, line 10-13), the LN optical phase modulator modulates the optical phase into π or 0 according to the value, 1 or 0, of an electrical signal to be input. And Wei et al teaches to use the output from the T-FF to drive the phase modulator. Since the "1" bit values in the sequence of the NRZ electrical signal have been separated into two groups, these two groups of driving signals will make the output optical signal with two phase 0 or π. That is the

combination of Ono and Kitajima and Wei et al will create "a device that generates an output having a phase that is correlated with the output of the T-flip-flop".

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1, and thus depending claims 1-6, recites the limitation "a T-flip-flop, having a first and second output port, for separating by received "1" bit values of the inputted NRZ electrical signal into first and second groups, wherein, said first group of "1" bit values has a first phase associated with a first output of the first output port and said second group of "1" bit values has a second phase associated with the second output of the first output port". However, the original disclosure does not disclose that the output from the T-flip flop has an associated phase, the output from the T-flip flop is the electrical signal; the phase of the optical signal is generated from the phase modulator.

6. Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1, and thus depending claims 1-6, recites the limitation "a T-flip-flop, having a first and second output port, for separating by received "1" bit values of the inputted NRZ electrical signal into first and second groups, wherein, said first group of "1" bit values has a first phase associated with a first output of the first output port and said second group of "1" bit values has a second phase associated with the second output of the first output port". However, the original disclosure does not teach how to make or use the T-flip flop that can generate an output with phase associated.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-6 and 9-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al (US 6,388,786) in view of Kitajima et al (US 5,515,196) and Wei et al (US 2002/0196508) and Kaiser et al (Kaiser et al, "Reduced Complexity Optical Duobinary 10-Gb/s Transmitter Setup Resulting in an Increased Transmission Distance", IEEE *Photonics Technology Letters, Vol. 13, No. 8, August 2001, pages 884-886*).

1). With regard to claim 1, Ono et al discloses a duobinary optical transmission apparatus (Figures 8, 13 and 23, ABSTRACT) comprising:

a light source (Semiconductor Laser 1 in Figure 8, 13 and 23) for outputting an optical carrier;

a Non-Return to Zero (NRZ) optical signal generating section (Optical Intensity Modulator 2 in Figures 8, 13 and 23) configured to receive an NRZ electrical signal, and for modulating the optical carrier from the light source into an NRZ optical signal according to said NRZ electrical signal (column 7, line 3-30); and

a duobinary optical signal generating section (Optical Phase Modulator 3 in Figures 8, 13 and 23) configured to receive said NRZ electrical signal and modulating said NRZ optical signal into a duobinary optical signal (column 7, line 10-30).

But, Ono et al teaches a precoder for processing the NRZ electrical signal, Ono et al does not expressly disclose the duobinary optical generating section comprises: a T-flip-flop, having a first and second output port, for separating by received “1” bit values of the inputted NRZ electrical signal into first and second groups, wherein, said first group of "1" bit values has a first phase associated with a first output of the first output port and said second group of "1" bit values has a second phase associated with the second output of the first output port.

However, the T-flip-flop circuit has been widely used in the art to precode or encode the inputted signal. Kitajima et al, in the same field of endeavor, teaches a T-flip-flop (Figure 8, column 9, line 55 to column 10 line 5), having a first output port (the

output 17-a in Figure 8A), for separating by received "1" bit values of the inputted NRZ electrical signal into first (see Figure O1, the shaded "1", e.g., shown in positions 1 and 3) and second groups (see Figure O1, the un-shaded "1", e.g., shown in position 2). Kitajima et al teaches that the T flip-flop 18-a is triggered in response to a **rise-up edge** of the input signal to thereby produce an output signal having a waveform such as illustrated in FIG. 8B at a row 2 (column 9 line 55-67), therefore, the odd group of "1" is separated into the "first group", and the even group of "1" is separated into the "second group"; and first group of "1" is "represented" by the electrical signal with intensity of "1" in the output of T-FF Q-Port, the second group of "1" is "represented" by the electrical signal with intensity of "0" in the output of T-FF Q-Port. And Wei et al also teaches a T-FF circuit to drive a phase modulator (Figure 16 and Figure 10, [0081]), and the T-FF has a first output port (the 1608 in Figure 16) and second output port (the 1610 in Figure 16), for separating by received "1" bit values of the inputted NRZ electrical signal into first and second groups (refer to the output 1608 in Figure 16).

And another prior art, Kaiser et al, discloses that by a toggle flip-flop (T-FF), no external feedback is required since the recursion is an integral function of the T-FF, and the T-FF structure using only feed forward building blocks avoids all problems with implementation and adjustment. Besides, an upgrade to higher bit rates of a single-chip integration can be done straightforwardly.

And, Ono et al also teaches a D Flip-Flop (D-FF) combined with a precoder. Ono et al uses the two outputs (Q and Q-bar) to drive a single optical modulator (e.g., Figures 18 and 22) to get both intensity modulation and phase modulation so to

generate a duobinary optical signal. It is well known to one skilled in the art that a T flip-flop can also be built using D flip-flop.

And Ono et al also teaches that the phase of the output signal from the duobinary modulators depends on the drive signal from the precoder and the phase different is 'π' (column 7, line 10-13, the LN optical phase modulator modulates the optical phase into π or 0 according to the value, 1 or 0, of an electrical signal to be input). And Wei et al teaches to use the output from the T-FF to drive the phase modulator. Therefore, it would be obvious to one skilled in the art to use the two outputs from a T-FF to drive the optical phase modulator, and then the first group of "1" bit values (or the odd group of "1") has a first phase (e.g., phase 0) associated with the output of the phase modulator and the second group of "1" bit values has a second phase (e.g., phase π) associated with the output of the phase modulator, so to obtain the duobinary signal. And, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the T-FF as taught by Kitajima et al and Wei et al and Kaiser et al to the system of Ono et al so that a simple structure T-FF without feedback tap can be obtained, and an upgrade to higher bit rates of a single-chip integration can be made easier.

2). With regard to claim 2, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claim 1 above. And Ono et al further discloses Ono et al further discloses wherein the light source comprises a laser diode (Semiconductor Laser 1 in Figure 8, 13 and 23).

3). With regard to claim 3, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claim 1 above. And Ono et al further

discloses wherein the NRZ optical signal generating section comprises a pair of first modulator driving amplifiers (Driving amplifiers 21 in Figure 15) for amplifying and outputting the NRZ electrical signal, and a first interferometer type optical intensity modulator (Optical Intensity Modulator in Figures 8, 13, 15 and 23) for modulating an intensity of said optical carrier according to driving signals inputted from said pair of first modulator driving amplifiers.

4). With regard to claim 4, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claims 1 and 3 above. And Ono et al further discloses wherein said first interferometer type optical intensity modulator comprises a Mach-Zehnder interference type optical phase modulator (Mach-Zehnder (MZ) Optical Intensity Modulator, column 7 line 4-5).

5). With regard to claim 5, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claim 1 above. And Ono et al further discloses wherein the duobinary optical generating section further comprises:

a pair of second amplifiers (Driving amplifiers 21 in Figure 15) for amplifying and outputting the signal from the precoder; and

a second interference type optical phase modulator (Optical Phase Modulator 3 in Figures 8, 13, 15 and 23) for modulating a phase of said NRZ optical signal according to driving signals from said pair of second amplifiers;

6). With regard to claim 6, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claim 1 above. And Ono et al further discloses wherein the NRZ optical signal generating section (Optical Intensity Modulator

2 in Figures 8, 13 and 23) is adapted for receiving the NRZ electrical signal from a pulse pattern generator (column 7, line 8-10).

7). With regard to claim 9, Ono et al further discloses a duobinary optical transmission apparatus comprising:

a light source (Semiconductor Laser 1 in Figure 8, 13, 15 and 23) for outputting an optical carrier;

a first modulator driving amplifier unit (Driving amplifiers 21 in Figure 15) for receiving, amplifying, and then outputting at least one NRZ electrical signal;

an optical intensity modulator(Optical Intensity Modulator in Figures 8, 13, 15 and 23) for modulating the intensity of the optical carrier according to a driving signal inputted from the first modulator driving amplifier unit;

a precoder (e.g., precoder 7 in Figures 8, 13, 15 and 23) for receiving the inputted NRZ electrical signal.

a second modulator driving amplifier unit (Driving amplifiers 21 in Figure 15) for amplifying and outputting at least one signal outputted from the precoder; and

an optical phase modulator (Optical Phase Modulator 3 in Figures 8, 13, 15 and 23) for modulating the phase of the NRZ optical signal according to at least one driving signal transmitted from the second modulator driving amplifier unit.

But, Ono et al teaches a precoder for processing the NRZ electrical signal, Ono et al does not disclose a T-flip-flop, having a first and second output port, separating '1' bit values of the NRZ electrical signal into first and second groups of "1" bit values, and after the phase modulator, wherein said first group of "1" bit values has a first phase

associated with a first output of the first output port and said second group of "1" bit values has a second phase associated with the second output of the first output port.

However, the T-flip-flop circuit has been widely used in the art to precode or encode the inputted signal. Kitajima et al, in the same field of endeavor, teaches a T-flip-flop (Figure 8, column 9, line 55 to column 10 line 5), having a first output port (the output 17-a in Figure 8A), for separating by received "1" bit values of the inputted NRZ electrical signal into first (see Figure O1, the shaded "1", e.g., shown in positions 1 and 3) and second groups (see Figure O1, the un-shaded "1", e.g., shown in position 2). Kitajima et al teaches that the T flip-flop 18-a is triggered in response to a **rise-up edge** of the input signal to thereby produce an output signal having a waveform such as illustrated in FIG..8B at a row 2 (column 9 line 55-67), therefore, the odd group of "1" is separated into the "first group", and the even group of "1" is separated into the "second group"; and the first group of "1" is "represented" by the electrical signal with intensity of "1" in the output of T-FF Q-Port, the second group of "1" is "represented" by the electrical signal with intensity of "0" in the output of T-FF Q-Port. And Wei et al also teaches a T-FF circuit to drive a phase modulator (Figure 16 and Figure 10, [0081]), and the T-FF has a first output port (the 1608 in Figure 16) and second output port (the 1610 in Figure 16), for separating by received "1" bit values of the inputted NRZ electrical signal into first and second groups (refer to the output 1608 in Figure 16).

And another prior art, Kaiser et al, discloses that by a toggle flip-flop (T-FF), no external feedback is required since the recursion is an integral function of the T-FF, and the T-FF structure using only feed forward building blocks avoids all problems with

implementation and adjustment. Besides, an upgrade to higher bit rates of a single-chip integration can be done straightforwardly.

And, Ono et al also teaches a D Flip-Flop (D-FF) combined with a precoder. Ono et al uses the two outputs (Q and Q-bar) to drive a single optical modulator (e.g., Figures 18 and 22) to get both intensity modulation and phase modulation so to generate a duobinary optical signal. It is well known to one skilled in the art that a T flip-flop can also be built using D flip-flop.

And Ono et al also teaches that the phase of the output signal from the duobinary modulators depends on the drive signal from the precoder and the phase different is 'π' (column 7, line 10-13, the LN optical phase modulator modulates the optical phase into π or 0 according to the value, 1 or 0, of an electrical signal to be input). And Wei et al teaches to use the output from the T-FF to drive the phase modulator. Therefore, it would be obvious to one skilled in the art to use the two outputs from a T-FF to drive the optical phase modulator, and then the first group of "1" bit values (or the odd group of "1") has a first phase (e.g., phase 0) associated with the output of the phase modulator and the second group of "1" bit values has a second phase (e.g., phase π) associated with the output of the phase modulator, so to obtain the duobinary signal. And, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the T-FF as taught by Kitajima et al and Wei et al and Kaiser et al to the system of Ono et al so that a simple structure T-FF without feedback tap can be obtained, and an upgrade to higher bit rates of a single-chip integration can be made easier.

8). With regard to claim 10, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claim 9 above. And Ono et al further discloses wherein each of the optical intensity modulator and the optical phase modulator comprises a Mach-Zehnder interferometer type optical modulator (Mach-Zehnder (MZ) Modulator, column 7 line 4-7).

9). With regard to claim 11, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claims 9 and 10 above. And Ono et al further discloses wherein the Mach-Zehnder interferometer type optical modulator is a dual-armed Z-cut Mach-Zehnder interferometer type optical modulator (Figure 15, the dual-armed Z-cut MZ modulators are used).

10). With regard to claim 12, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claims 9-11 above. And Ono et al further discloses wherein each of the first and second modulator driving amplifier units includes a pair of modulator driving amplifiers (Driving amplifiers 21 in Figure 15), each of which amplifies the NRZ electrical signal inputted to itself.

11). With regard to claim 13, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claims 9 and 10 above. And Ono et al further discloses wherein the Mach-Zehnder interferometer type optical modulator is a single-armed X-cut Mach-Zehnder interferometer type optical modulator (e.g., Figure 8, the Mach-Zehnder modulator is the LN X-cut single-armed modulator).

12). With regard to claim 14, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claim 9 above. And Ono et al

in view of Kitajima et al and Kaiser et al discloses wherein the first group of `1` in the sequence and the second group of `1` in the sequence have been separated from the NRZ electrical signal, respectively (Ref to Figure O1).

But, Ono et al does not expressly disclose wherein the first group of `1` bit values in the sequence and the second group of `1` bit values in the sequence have a phase difference of 'π' with respect to each other.

As shown in Figure O1, Kitijma et al and Wei et al teaches that the T-flip-flop separating by received "1" bit values of the inputted NRZ electrical signal into first (see Figure O1, the shaded "1", e.g., shown in positions 1 and 3) and second groups (see Figure O1, the un-shaded "1", e.g., shown in position 2), that is, the group of `1` in odd positions in the sequence and the group of `1` in even positions in the sequence are separated from the NRZ electrical signal, respectively; and first group of "1" is "represented" by the electrical signal with intensity of "1" in the output of T-FF Q-Port, the second group of "1" is "represented" by the electrical signal with intensity of "0" in the output of T-FF Q-Port. And Ono et al also teaches that the phase of the output signal from the duobinary modulators depends on the drive signal from the precoder and the phase different is 'π' (column 7, line 10-13, the LN optical phase modulator modulates the optical phase into π or 0 according to the value, 1 or 0, of an electrical signal to be input). And Wei et al teaches to use the output from the T-FF to drive the phase modulator. Refer to Figure O1, the drive signal for the first group is different from the drive signal for second group, therefore, it would be obvious that the first group of

`1` in the sequence and the second group of `1` in the sequence have a phase difference of 'π' with respect to each other.

13). With regard to claim 15, Ono et al discloses a method for duobinary optical transmission comprising the steps of:

(a) outputting a light source as an optical carrier (Semiconductor Laser 1 outputs a light source, Figure 8, 13 and 23);

(b) receiving an NRZ electrical signal (Optical Intensity Modulator 2 receives an NRZ electrical signal, Figures 8, 13 and 23) and modulating the optical carrier from the light source into an NRZ optical signal according to said NRZ electrical signal by providing a Non-Return to Zero (NRZ) optical signal generating section (column 7, line 3-30); and

(c) receiving said NRZ electrical signal (Optical Phase Modulator 3 receives NRZ electrical signal, Figures 8, 13 and 23) and modulating said NRZ optical signal into a duobinary optical signal by a duobinary optical signal generating section signal (column 7, line 10-30), each phase associated with a phase generating signal (column 7, line 1—13, the LN optical phase modulator modulates the optical phase into π or 0 according to the value, 1 or 0, of an electrical signal to be input).

But, Ono et al teaches a precoder for processing the NRZ electrical signal, Ono et al does not expressly disclose separating '1' bit values in the sequence of the NRZ electrical signal into a first and second group of '1' bit values, and the duobinary optical signal generating section associates each element of said first group of '1' bit values

with a first phase and each element of said second group of '1' bit values with a second phase.

However, Kitajima et al, in the same field of endeavor, teaches a T-flip-flop (Figure 8, column 9, line 55 to column 10 line 5), for separating "1" bit values in the sequence of the NRZ electrical signal into first (see Figure O1, the shaded "1", e.g., shown in positions 1 and 3) and second (see Figure O1, the un-shaded "1", e.g., shown in position 2) groups of '1' bit values. Kitajima et al teaches that the T flip-flop 18-a is triggered in response to a **rise-up edge** of the input signal to thereby produce an output signal having a waveform such as illustrated in FIG. 8B at a row 2 (column 9 line 55-67), therefore, the odd group of "1" is separated into the "first group", and the even group of "1" is separated into the "second group"; and first group of "1" is "represented" by the electrical signal with intensity of "1" in the output of T-FF Q-Port, the second group of "1" is "represented" by the electrical signal with intensity of "0" in the output of T-FF Q-Port. And Wei et al also teaches a T-FF circuit to drive a phase modulator (Figure 16 and Figure 10, [0081]), and the T-FF has a first output port (the 1608 in Figure 16) and second output port (the 1610 in Figure 16), for separating by received "1" bit values of the inputted NRZ electrical signal into first and second groups (refer to the output 1608 in Figure 16).

And another prior art, Kaiser et al, discloses that by a toggle flip-flop (T-FF), no external feedback is required since the recursion is an integral function of the T-FF, and the T-FF structure using only feed forward building blocks avoids all problems with

implementation and adjustment. Besides, an upgrade to higher bit rates of a single-chip integration can be done straightforwardly.

And Ono et al also teaches that the phase of the output signal from the duobinary modulators depends on the drive signal from the precoder and the phase different is 'π' (column 7, line 10-13, the LN optical phase modulator modulates the optical phase into π or 0 according to the value, 1 or 0, of an electrical signal to be input). And Wei et al teaches to use the output from the T-FF to drive the phase modulator. Therefore, it would be obvious to one skilled in the art to use the two outputs from a T-FF to drive the optical phase modulator, and then each element of the first group of "1" bit values (or the odd group of "1") has a first phase (e.g., phase 0) and each element of the second group of "1" bit values has a second phase (e.g., phase π), so to obtain the duobinary signal. And, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the T-FF as taught by Kitajima et al and Wei et al and Kaiser et al to the system of Ono et al so that a simple structure T-FF without feedback tap can be obtained, and an upgrade to higher bit rates of a single-chip integration can be made easier.

14). With regard to claim 16, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claim 15 above. And Ono et al further Ono et al further discloses wherein the light source used in step (a) comprises a laser diode (Semiconductor Laser 1 in Figure 8, 13 and 23).

15). With regard to claim 17, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claim 15 above. And Ono et

al further discloses wherein the NRZ optical signal generating section used in step (b) comprises a pair of first modulator driving amplifiers (Driving amplifiers 21 in Figure 15) for amplifying and outputting the NRZ electrical signal, and a first interferometer type optical intensity modulator (Optical Intensity Modulator in Figures 8, 13, 15 and 23) for modulating an intensity of said optical carrier according to driving signals inputted from said pair of first modulator driving amplifiers.

16). With regard to claim 18, Ono et al and Kitajima et al and Wei et al and Kaiser et al disclose all of the subject matter as applied to claim 15 above. And Ono et al further discloses wherein said first interferometer type optical intensity modulator comprises a Mach-Zehnder interference type optical phase modulator (Mach-Zehnder (MZ) Optical Intensity Modulator, column 7 line 4-5).

17). With regard to claim 19, Ono et al and Kitajima et al and Wei et al and Kaiser et al discloses all of the subject matter as applied to claim 15 above. And Ono et al and Kitajima et al and Wei et al and Kaiser et al further teach wherein the duobinary optical generating section used in step (c) comprises a T-flip-flop for generating said phase generating signal from said inputted NRZ electrical signal (Kitajima et al Figure 8 and Wei et al Figure 16 teach the T-flip-flop circuit to generate the phase generating signal); a pair of second amplifiers (Ono et al: Driving amplifiers 21 in Figure 15) for amplifying and outputting the signal from the precoder; and a second interference type optical phase modulator (Ono et al: Optical Phase Modulator 3 in Figures 8, 13, 15 and 23) for modulating a phase of said NRZ optical signal according to driving signals from said pair of second amplifiers.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li Liu whose telephone number is (571)270-1084. The examiner can normally be reached on Mon-Fri, 8:00 am - 5:30 pm, alternating Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on (571)272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Li Liu
February 8, 2008

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER